

LOW DISTORTION SIGNAL GENERATOR BASED ON DIRECT DIGITAL SYNTHESIS FOR ADC CHARACTERIZATION

Walter F. Adad¹, Ricardo J. Iuzzolino¹

¹ Instituto Nacional de Tecnología Industrial, Buenos Aires, Argentina, adad@inti.gov.ar

Abstract: This paper presents a low distortion signal generator with a frequency range from 0 to 10 kHz using the direct digital synthesis (DDS) method for ADC characterization. The results show that the maximum distortion in the whole frequency range is -80.37 dB, the frequency resolution is 1.421 nHz (with a 48-bits DDS chip), the stability in frequency is 25 μ Hz/Hz and the amplitude stability is 13 μ V/V.

Key words: direct digital synthesizer, frequency synthesizers, direct digital synthesis, function generator.

1. INTRODUCTION

Analog to digital converters (ADC) and digital to analog converters (DAC) have to be characterized in a static and dynamic regime.

Static characterization can be made using a solid state DC voltage standard or a Josephson system. While, for dynamic characterization, it is necessary to excite the ADC with different types of signals waveforms, amplitudes and frequencies. To attack these problems we have designed an arbitrary function generator based on direct digital synthesis (DDS) method. This digital method offers advantages over the phase locked loop (PLL), which are mentioned below:

- High resolution in the output frequency.
(There are commercial devices with 32 and 48 bits which allow achieving a frequency resolution in the order of the nHz).
- Low transient time to the output frequency.
- High usable frequency range.
- Low phase noise.
- Little space requirements.

(Commercial DDS devices have small packaging and the solutions are given by software).

This function generator can be used in other applications such as time and frequency measurements, calibration of sound level meters, calibration of electrocardiographs, impedance measurements (as described in [1]) and any measurement schemes which require alternating signals as a stimulus.

2. THEORY OF OPERATIONS OF DIRECT DIGITAL SYNTHESIS

DDS technique consists in digital processing to generate signals at different frequencies and phases selectable by software, from a reference clock.

As the DDS technique consists in dividing the reference clock frequency from a tuning word selectable by software,

the relationship between the tuning word, the clock reference, the number of bits of the DDS and the desired output signal frequency is given by [2]:

$$f_o = M \frac{f_{\text{clock}}}{2^N} \quad (1)$$

where f_o is the output frequency, M is the tuning word, f_{clock} is the reference clock frequency and N is the phase accumulator resolution.

Replacing $M = 1$ in equation (1) gives the frequency resolution, f_r , of the DDS devices as:

$$f_r = \frac{f_{\text{clock}}}{2^N} \quad (2)$$

For example, with a 48 bits DDS and a reference clock of 400 kHz it is possible to obtain a frequency resolution of 32.52 nHz.

A simplified blocks diagram of DDS device is depicted in Figure 1. The blocks diagram consists of four blocks: a reference clock, a phase accumulator, a look-up table and a D/A converter.

The phase accumulator sums at each clock pulse the tuning word. Thus, its output is a digital ramp (binary code), as shown in Figure 1.

The look-up table converts the phase accumulator output to a digital sinusoidal waveform.

Because of limitations in the number of bits of the look-up table, the high resolution output of the phase accumulator (32 or 48 bits) is truncated. This truncation introduces spurious components in the output signal spectrum that must be filtered in order to obtain low distortion.

Finally, the D/A converter transforms the digital sinusoidal waveform into an analog signal. The nonlinearities of the D/A converter are the major source of harmonic distortion.

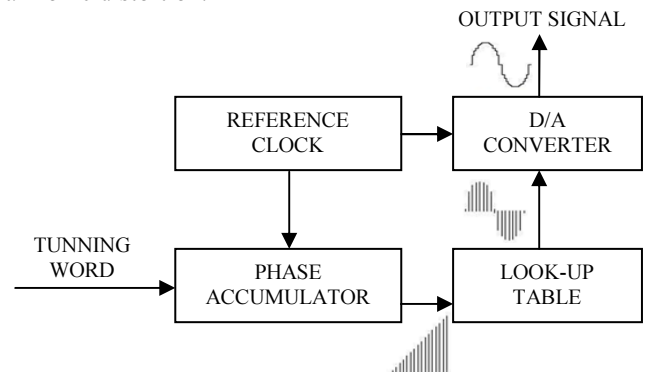


Fig 1. DDS's simplified block diagram.

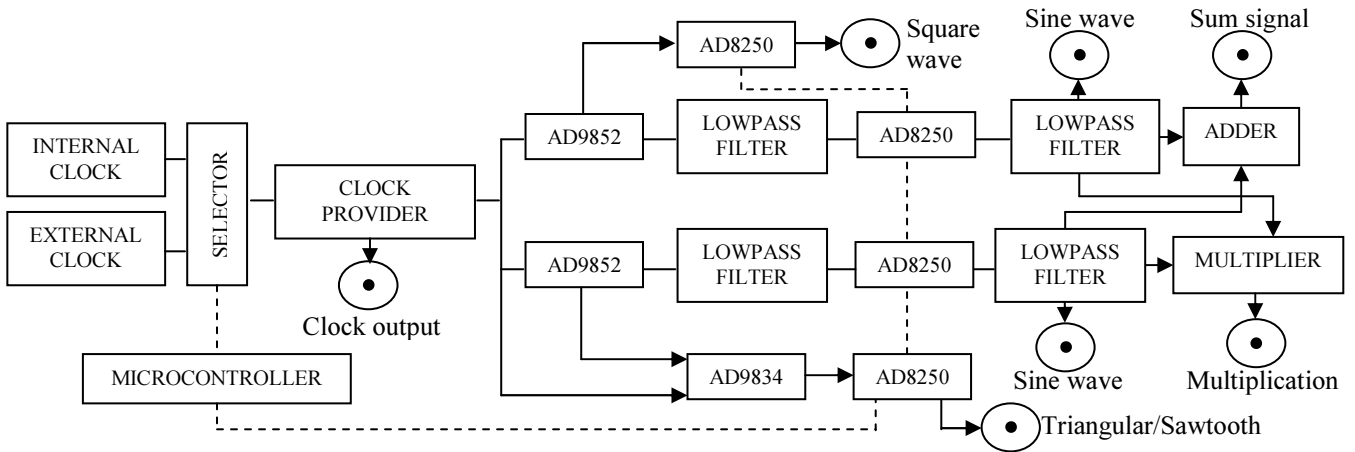


Fig 2. Simplified block diagram of the complete system

2. SYSTEM DESCRIPTION

Figure 2 shows a simplified block diagram of the complete system.

Internal clock and external clock blocks in the diagram represent the reference clock. The clock selector allows choosing between the internal clock (a quartz crystal) and an external clock. This clock selector is controlled by a microcontroller. Since the DDS technique does not introduce frequency instability to the system, the stability in frequency is dominated by the internal or external clock.

The clock provider block delivers the clock signal to the system and also provides an external output for synchronization with other systems.

The system generates single-tone, multi-tone, triangular, saw-tooth and square waveform signals. To generate dual tone signals, two AD9852 devices are used, while to generate single-tone signals, one of them can be used.

Since the AD9852 are only capable of generating sine and square waveforms, a third DDS was added, the AD9834, to generate triangular and saw-tooth waveforms.

To generate the triangular waveform, the AD9834 internally bypasses the look-up table and directly connects the phase accumulator output to the DAC.

On the other hand, to generate the saw-tooth waveform, as suggested in [3], pulses generated by the AD9852 switch between the phase of the two triangular waveforms produced by the AD9834. Figure 3 illustrates this situation.

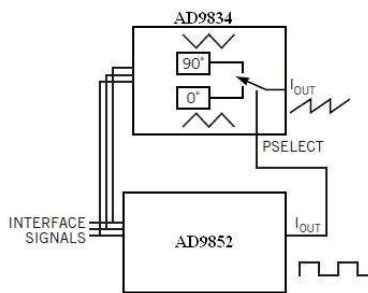


Fig 3. Simplified block diagram of the sawtooth waveform generation.

As it has been described in last section the digital output signal must be filtered. Therefore, Butterworth low pass passive filters of third order with a cutoff frequency of 20 kHz were placed at the output of the AD9852. As in [4], they were implemented with passive components so that the only noise source is the thermal noise introduced by resistors. The Butterworth topology was used because of the flatness in the passband.

To generate different amplitudes of the output signals, low distortions Programmable Gain Amplifier (PGA) were employed, the AD8250. The gain can be set to 1, 2, 5 or 10.

Next to the low distortion amplifiers, lowpass filters were placed (in the case of sinusoidal signal) to remove spurious frequencies generated by the PGA. They have the same topologies of the first one, but with a cutoff frequency of 100 kHz.

Finally there are an adder and a multiplier circuits to generate the dual tone signals. AD734AN is used as multiplier because of its low distortion.

SOURCES OF DISTORTION

In order to evaluate the DDS behavior, the main distortion sources were analyzed which are:

- Phase accumulator truncation.
- Internal D/A converter.
- Interference between tracks in the PCB design.

To simulate and validate the performance of the system a simulation program was developed. Simulation results have shown that the spurious frequency due to phase accumulator truncation were over the bandwidth of the system (10 kHz), and can be filtered properly with the filters mentioned in the previous section. These reconstruction filters, also reduce the harmonic distortion caused by the D/A converter.

To reduce the quantization noise effects, different measurements were performed in the system. Some of these measurements are showed in section 3 and they consist of varying the relationship between the DDS output frequency and the reference clock frequency.

The PCB was designed to reduce interference between tracks, as suggested in [5] and [6]. The following issues were taken into account:

- Ground plane inclusion.

A two layers PCB was designed. The bottom layer as a ground plane. With its inclusion the THD has been reduced in 10 dB.

- Capacitive crosstalk reduction.

To reduce the interference between tracks, we tried to avoid parallel tracks, keeping them as short as possible.

- DDS's AD9852 synchronization.

The generation of dual-tone signals employs two AD9852 devices synchronized. To accomplish that, the tracks from the reference clock to these devices were routed with the same length.

- Reference clock low impedance return path.

Tracks crosses behind the track of the reference clock (bottom layer) were avoided in order to prevent the spread of the return current throughout the circuit.

3. RESULTS

To verify the system behavior, different types of tests were carried out. As described in the following sections.

3.1 Influence of reference clock frequency on the output signal spectrum

This test consisted of configure the DDS to generate a determinate frequency (1 kHz) and vary the reference clock frequency. It was performed to select the best frequency of the reference clock. Thus, the total harmonic distortion (THD) was calculated at different reference clock frequencies. Table 1 shows us that reducing the bandwidth of the system imply a THD reduction.

Table 1. THD at different f_{REFCLK} , f_o ratios.

DDS frequency output	Clock reference frequency	$\frac{f_{REFCLK}}{f_o}$	THD
1 kHz	20 MHz	20000	-77.87 dB
1 kHz	100 kHz	100	-80.37 dB
1 kHz	80 kHz	80	-80.57 dB

An improvement of 2.5 dB was obtained when the ratio between the reference clock frequency and the output frequency is reduced from 20000 to 100. When this ratio was set to 80, the THD was reduced in 2.7 dB.

3.2 Influence of multiple output frequency of the reference clock frequency

First, the DDS was programmed to generate an output frequency which is multiple of the reference clock. After that, the DDS was programmed to generate an output frequency which is not multiple of the reference clock.

The results are shown in table 2.

Table 2. THD as function of DDS output frequency.

DDS output frequency	Clock reference output frequency	THD
1000 Hz	80 kHz	-80.57 dB
1001.457 Hz	80 kHz	-80.77 dB

These results show an improvement of 0.2 dB in the THD when the output signal frequency was not an integer multiple of the reference clock frequency.

3.2 Internal frequency multipliers

The AD9852 has an internal frequency multiplier with which is possible to increase the frequency of the reference clock.

To evaluate the influence of this frequency multiplier on the THD, the DDS was programmed to generate the same output frequency using different multiplier settings. Then the THD was obtained.

The results are depicted in table 3.

Table 3. Influence of multiplier in the THD.

DDS output frequency	Clock reference output frequency	Multiplier	THD
1 kHz	80 kHz	x5	-80.16 dB
1 kHz	100 kHz	x4	-80.16 dB

It is important to point out that the DDS internal frequency was the same at both cases (400 kHz). As can be seen in table 3, no changes were observed in the THD at different values of the DDS internal multiplier, therefore there are not variations of the THD as a function of the multiplier.

3.1 Frequency and amplitude stability

To analyze the frequency and amplitude stability of the system the DDS was programmed to generate a sinusoidal waveform of 62.5 Hz. The frequency was measured connecting directly the DDS output signal to a time interval counter. The amplitude was measured with a digital multimeter.

The measurement results of the frequency and amplitude stability are shown in Table 4.

Table 4. Frequency and amplitude stability of the DDS output .

Frequency stability	Amplitude stability
25 μ Hz/Hz	13 μ V/V

The Allan deviation of the DDS output signal frequency when the internal clock was used is illustrated in figure 4. This figure shows that an observation time in the range of 20 s to 16000 s can be employed because of the predominant noise in the whole range is white noise, as described in [7].

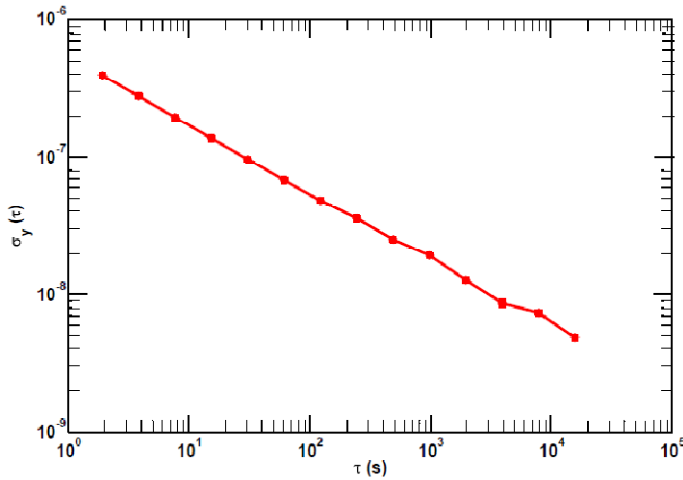


Fig 4. Allan deviation of the DDS frequency output signal.

Figure 5 shows the Allan deviation of the output signal amplitude. To achieve the optimal $\sigma_y(\tau)$, an observation time (τ) of 15.25 s has to be used, as suggested in [7].

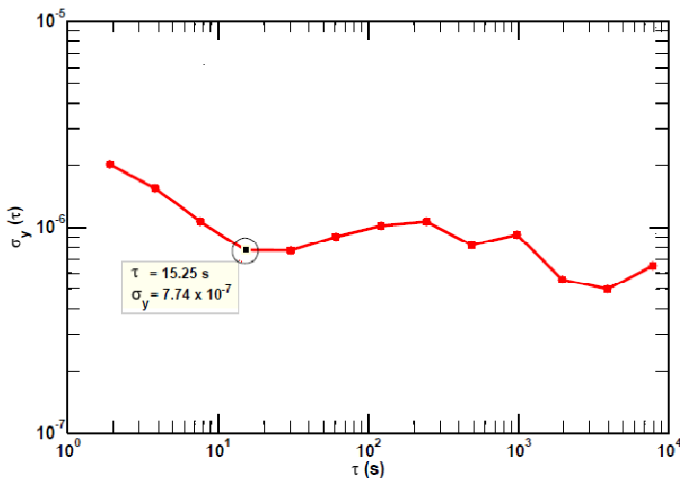


Fig 5. Allan deviation of the DDS amplitude output signal.

3.2 Total harmonic distortion

Figure 6 shows the measurement of the DDS output spectrum when it was programmed to generate an output signal of 1 kHz. Figure 7 shows the simulation of the DDS output spectrum considering an output signal of 1 kHz.

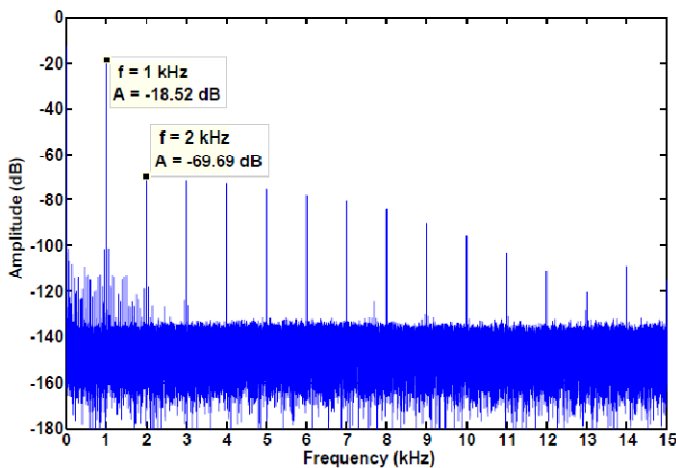


Fig 6. DDS Output spectrum obtained by measurement.

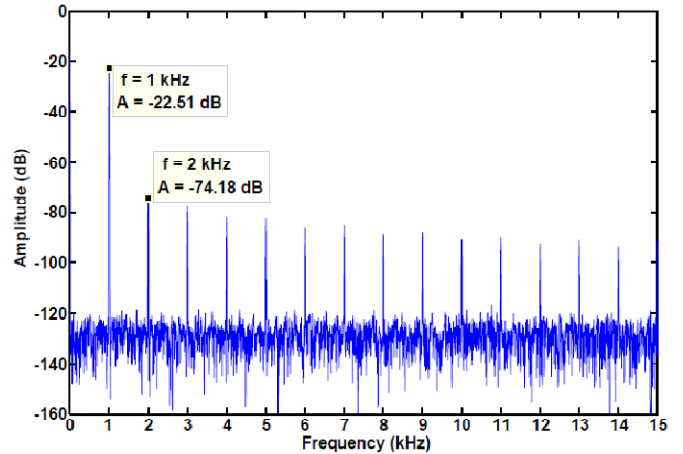


Fig 7. DDS Output spectrum obtained by simulation.

By measurement we obtained a SFDR = -57.17 dBc while by simulation we obtained a SFDR = -51.67 dBc. It is important to point out that this is due to a reconstruction filter was not applied in order to evaluate the DDS behavior.

After the application of a reconstruction filter, the maximum simulated and measured THDs are summarized in Table 5.

Table 5. Maximum Total Harmonic Distortion of the system.

THD by simulation	THD by measurements
-80.62 dB	-80.37 dB

From these results it is possible to observe that the simulation program and the measurement are in agreement within 0.25 dB. As a consequence, the simulation program can be used to validate the performance of the system.

4. CONCLUSION

We designed a low distortion (-80.37 dB) arbitrary function generator with a resolution equal to 1.41 nHz and frequency stability of 25 μ Hz/Hz.

In addition, a simulation program for the AD9852 was developed. This program allowed us to evaluate the DDS behavior.

Since the direct digital synthesis technique is based on digital signal processing it does not introduce instability to the frequency. Therefore, the only contribution to the frequency uncertainty is the relative uncertainty of the reference crystal. As the system has the possibility to connect an external reference clock, the achievable stability can be improved. This feature is useful, for example, to adjust frequencies in time and frequency measurements.

This function generator may be used in electrical metrology, in any scheme of measurements that require AC signals as a stimulus.

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