



# Investigations on an extended high speed data-interface for image processing using Field Programmable Gate Array based on embedded processing

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**Abstract:** The main focus in this paper lies on a novel interface design to transmit image data combined with results through a single interface. Therefore the data stream is divided in two logical parts the image data and the result data. The big advantage is the transfer via different standardized interfaces like Universal Serial Bus (USB) or Gigabit-Ethernet (GigE) Vision. The transfer model was tested in a scalable hardware platform developed in previous work.

**Key words:** high speed data interface, real time image processing, FPGA based embedded processing

## 1. State of the art for image processing technologies and camera based data transfer

Image processing in embedded platforms is more important as never before. That depends on the continuous growing of sensor sizes and readout frequency in the last years. The trend is structured into the DSP (Digital Signal Processor) based Designs and the FPGA based Designs. Furthermore there is a trend in combined FPGA-DSP systems [1], which gains the importance of that field of embedded image processing.

Typically industrial embedded image processing systems are programmed over specific software of the manufacturer on a host PC. Deep-going interventions into the camera configuration are not intended. Beyond that the user is fixed on firm program modules. After programming the program will transfer to the camera, which thereupon works independently. For programming purpose, mostly a slow interface like RS 232 or Ethernet 10/100 Mbit is applied. It is not necessary in most cases to receive image information in form of a live stream. Computational results are transmitted through the same interface. In most application, no additional data bandwidth is needed, because the whole computation/processing is realized in the camera [2].

These solutions working well for teach-in modes and low result data rates. Some camera systems provide an additional analogue output to support user observation during programming process. For high-dynamic reconfigurable applications of filters or applications in those embedded systems accomplishes only fast preprocessing functions, additionally also the image information is needed at the same time. With state of the art systems this is not possible. Therefore a new tunable data interface will be presented.

## 2. Introduction in the scalable hardware platform

The concept of a scalable hardware platform was presented in [3]. The system consists of three hardware layers: the data acquisition layer, an embedded processing layer and the data transmission layer. Actually it was extended with a multipurpose layer. The layers are described in the following sections.

### 2.1. Data acquisition layer board

The data acquisition layer board (DALB) generates the raw image data. Two types of optoelectronic sensors are realized, the CCD types and the CMOS types. During the hardware development cycle a consistent internal interface was developed. It contains the image data signals with reference signals and beyond that additional external control signals, for example a asynchronous reset signal. For the sensor configuration, the interface include a inter integrated circuit (I<sup>2</sup>C) bus. Supported imaging sensor devices are listed in Table 1:

Table 1. Overview about realized data acquisition layer boards.

Sensor Model	Format	Type
Sony ICX 424AL	640 x 480	CCD
Sony ICX 415AL	768 x 576	CCD
Sony ICX 204AL/AQ	1024 x 768	CCD
Aptina MT9V034	752 x 480	CMOS
Aptina MT9M001	1280 x 1024	CMOS
Aptina MT9T031	2048 x 1536	CMOS

The hardware realization is done by a unique interface header which carries out these signals.

### 2.2. Embedded processing layer board

The embedded processing layer board (EPLD) is switched between the data acquisition layer board and the transmission layer board. It takes over the data processing for the high speed interface. The outside interfaces correspond to those of the acquisition layer board. The image data stream flowing through the logic and can be influenced. Actually three types of plug-in boards are available and tested. Table 2 shows the main features of the boards.

Table 2. Key features of the available embedded processing layer boards.

Board type	FPGA	Key features
S3ADSP-1800	Xilinx Spartan 3A-DSP XC3SD1800A	16.640 Slices 84 x DSP48A 1512 kBit Block RAM
S3E-500	Xilinx Spartan 3E XC3S500E	4.656 Slices 360 kBit Block RAM
S3E-1200	Xilinx Spartan 3E XC3S1200E	8.672 Slices 504 kBit Block RAM

The processor in form of an FPGA offers sufficient arithmetic performance to take over different computation and preprocessing tasks. Apart from the realization of typical image processing filters as simple manipulation of the image data [4] also computations can take place from picture contents [5].

### 2.3. Transmission Layer board:

The data transmission layer board (TLB) is likewise connected by the internal interface with the embedded processing layer board. The transmission of valid image data is accomplished on basis of the image reference signals. As long as the format corresponds to a valid data frame, the kind of the transmitted data is unimportant. Actually a USB interface is used to transmit the data. In the future a GigE-Vision interface is planned to spread the bandwidth.

## 3. NEW CONCEPT FOR THE INTERFACE

In order to fulfill the demand of the transmission of live image data and parallel computation results, the data transmission had to be extended. For this purpose the special characteristics of the raw image data stream were used. Apart from the actual image information the signal contains horizontal and vertical blanking. These dead times are leftovers of the analogue display on cathode ray tube monitors. Their length is specified by the image reference signals. These times can be used by faster processors, in order to convey additional information. This works like the embedded videotext data in the analogue television signal. The image data and the results will be filtered in the host PC.

### 3.1. Theoretical system concept embedded part

Based on the target hardware platform described in part two of this paper, this section describes the approach. For the development of this new interface two constructs were build in different kind of software structures. The embedded processing layer receives the data from the acquisition layer and buffering some lines of the current image. After receiving the required amount of lines of valid real image pixels the image processing algorithm starts its calculation. Finishing the processing of the first line a block of result data is attached to the first line of valid image data. If the data coupling is finished a new timing must be generated in the embedded layer to transmit the mixed data to the data transfer layer. Therefore the maximum time slit, respective the maximum transferable image data combined with result data, depending on the timing of the CCD or CMOS Sensor. It is exactly the time between the last image pixel and the

next vertical line signal. The time gap between the first incoming sample and the first outgoing sample depends on the complexity of the image processing algorithm (Fig. 1).

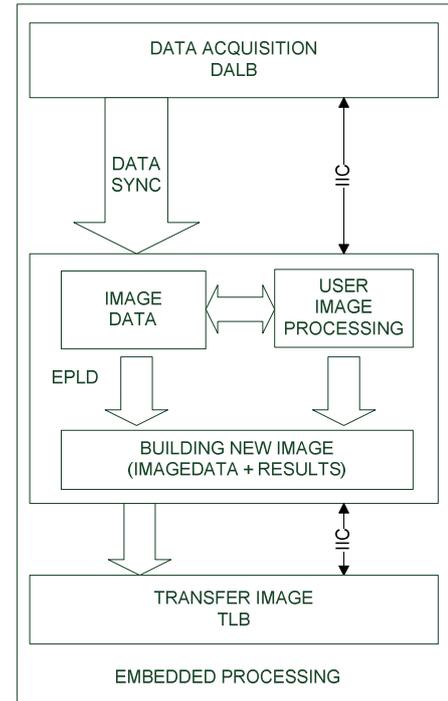


Fig. 1. Data flow in the embedded system

### 3.2. Theoretical system concept PC part

After the transfer is done through the transmit layer the mixed data will be received by the PC. To filter the data into image and result data a dynamic link library was developed. The algorithm in this library allocates the needed memory for the two data blocks and pass over the data pointer to the user application. After that the user can display the data or can organize additional processing. Figure 2 illustrates that process.

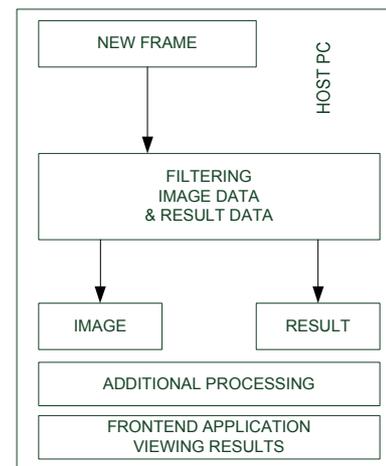


Fig. 2. Filtering and data processing in the host pc

## 5. TEST SETUP AND RESULTS

To verify the theoretical constructs a setup of the three layers were combined together in a hardware stack. For the

embedded processing the Spartan FPGA S3ADSP-1800 was used. The transmission layer was realized by an USB transmitter device. So the maximum theoretical bandwidth is limited up to 480 MBit/s. For the example application a VGA sensor resolution was required. Therefore the Aptina MT9T031 sensor in binning operation modus was the test circuit. According to the sensor timing the image size of 740x480 pixel is possible. The VGA valid pixel format is 640x480 pixel. That leads to a data rate of visible pixel (product of sensor size, data resolution and frame rate):

$$640*480*8\text{Bit}*60(\text{fps}) = 147,456 \text{ Mbit/s} \quad (1)$$

And a result data rate which is transferred in the horizontal blanking of:

$$100*480*8\text{Bit}*60(\text{fps}) = 23,04 \text{ Mbit/s} \quad (2)$$

In sum the sum data rate of image data and result data is calculated by

$$147,456 \text{ Mbit/s} + 23,04 \text{ Mbit/s} = 170,496 \text{ Mbit/s} \quad (1+2)$$

In the tested setup a payload of 23,04 Mbit/s can be achieved. Increasing the payload rate leads to instability in the image data. The theory of the embedded concept was proofed with this setup.

## 5. CONCLUSION

In this paper a possibility for transmitting data trough an image live stream was discussed. Therefore a hardware layer stack was developed and used to proof the concept. Furthermore a software concept shows the filtering of the mixed data on the host pc. This setup was needed to divide the data processing into a part of preprocessing in the hardware and a part of processing in the host pc software. This realization was used to monitoring the processing in the hardware platform on the pc to debug some error cases. It is well suited for developers integrating data processing in FPGA devices. A detailed description of the VHDL constructs and the timing problems during the realization will be given in the complete paper.

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## REFERENCES

- [1] Xilinx Inc., "Processor-centric extensible platforms for powerful, scalable, cost-efficient embedded designs", product brief ZYNQ 7000 EPP
- [2] Vision&Control GmbH, "vcwin 2.9", user manual, 2011 Suhl, Germany.

- [3] M. Rosenberger, M. Schellhorn, M. Correns, M. Schumann, M. Vogel, G. Linss, "An novel approach for teaching digital image processing based on an new multi-scalable hardware platform", Proceedings of the XIX IMEKO World Congress Fundamental and Applied Metrology, September 6-11, 2009, Lisbon, Portugal.

- [4] M. Schellhorn, M. Rosenberger, M. Correns, M. Blau, A. Göpfert, M Rückwardt, G. Linss "Field programmable gate array based hardware implementation of a gradient filter for edge detection in colour images with subpixel precision", Proceedings of the 55th International Scientific Colloquium, September 13-17, 2010, Ilmenau, Germany.

- [5] P. Husar, F. Klefenz, "Fraunhofer eye tracker - a calibration free solution with scalable and configurable Hough IP Core", Fraunhofer Institute for Digital Media Technology IDMT entry for the Vision Award 2010, fair guide Vision 2010, November 9-11, 2010, Stuttgart, Germany.